Amendments to the Claims

1. (canceled)

2. (currently amended) A memory system, comprising:

at least two ferroelectric polymer memory devices arranged such that a control signal output from one device is electrically connected to a control signal input to a sequential device, such that the control signal is asserted at the devices in series and the devices have busy signal to indicate when the devices are responding to the control signal.

3. (original) The memory system of claim 2, wherein each memory device further comprises a address latch and a data latch, operable to temporarily hold address and data signals.

4. (original) The memory system of claim 2, the memory system further comprising a system controller to generate an initial data in control signal for a first memory device.

5. (original) The memory system of claim 4, the memory system further comprising a data bus to transfer data between each memory device and the system controller

6. (original) The memory system of claim 2, the memory system further comprising an address bus to provide addressing of the memory devices.

7. (original) The memory system of claim 4, wherein the system controller is also operable to receive a data out control signal from a last device.

8. (original) A method of performing a read operation on at least two ferroelectric memory devices linked sequentially, the method comprising:

detecting a busy signal from a selected one of the memory devices to which an address has been transmitted;

asserting an input control signal for the selected one of the memory devices;

receiving data from the selected one of the memory devices; and

asserting an output control signal from the selected one, wherein the output control signal provides an input control signal to an adjacent memory device.

9. (original) The method of claim 8, the method comprising repeating the detecting, asserting, receiving and asserting processes until all of the memory devices have been selected.

10. (original) The method of claim 8, wherein the method further comprises sending an address for a new read operation before all data has been received from all devices.

11. (original) A method of performing a write operation on at least two ferroelectric memory devices linked sequentially, the method comprising:

receiving an input control signal from a system controller at a selected one of the ferroelectric memory devices;

asserting a busy signal after data has been received at the selected one;

asserting an output control signal; and

receiving data from the system controller at each of the memory devices until all memory arrays have received their data.

12. (original) The method of claim 11, wherein receiving data from the system controller further comprises a continuous stream of data on the data bus.

13. (original) A memory device, comprising:

a ferroelectric polymer memory array; and

device control circuitry operable to receive and send control signals such that an output control signal is transmitted to an adjacent memory device as an input control signal, the control signals including a busy signal receivable from the ferroelectric polymer memory array.

14. (original) The memory device of claim 13, the device comprising an address latch an address latch to temporarily store addresses for memory operations.

15. (original) The memory device of claim 13, the device comprising a data latch to temporarily store data.

16. (original) The memory device of claim 14, the device control circuitry further to direct the address latch to receive address signals.

17. (original) The memory device of claim 15, the device control circuitry further to direct the data latch to receive and send data signals.

18. (original) The memory device of claim 13, wherein the control signals include a serial data in control signal and a serial data out control signal.